**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (original) A system comprising:

a transmitter board for transmitting a copy of signals produced in such system, the copy of such signals comprises serial data in a low byte serial link and in a high byte serial link, the signals include special characters interspersed in a pattern with the data in the low and high byte serial links;

a system analyzer board comprising:

a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board, and for converting the received data and the special characters interspersed in both the low and high byte serial links into corresponding data and the interspersed special characters in low byte and high byte parallel links; and

a logic for determining mismatches between the data and the interspersed pattern of special characters in the converted low byte parallel link and the converted high byte parallel link and for producing a reset signal for the serializer-deserializer when a predetermined plurality of mismatches is determined.

2. (currently amended) The system recited in claim 1 wherein the logic maintains a count of the number of mismatches, such system providing ~~a~~ the reset signal to the serializer-deserializer when a predetermined plurality of mismatches has been indicated.

3. (currently amended) A system analyzer, comprising;

a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data, each such

data being in a series a low byte serial link and a high byte serial link, such signals including with the data and special characters interspersed in a pattern with the data in the low byte serial link and interspersed with the data in such high byte serial link;

an analyzer board adapted for plugging into the transmitter board, such analyzer board comprising:

a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board, and for converting the received data and the special characters interspersed therewith in the low byte serial link into corresponding a low byte parallel link and concurrently converting the received data and the special characters interspersed therewith in the ~~low~~ high byte serial link into a corresponding high byte parallel link;

a system for determining whether the data and interspersed pattern of special characters in the converted low byte parallel link mismatch the data and the interspersed pattern of special characters in the converted high byte parallel link, a determined mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches, such system providing a reset signal to the serializer-deserializer when a predetermined plurality of mismatches has been indicated.

4. (currently amended) A system analyzer, comprising;

a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data, each such data in the series having lower significant bytes thereof in a low byte serial link and having more significant bytes thereof in a high byte serial link, such signals including with the data, special characters interspersed in a pattern with the bytes of each of the data in such low byte serial link and interspersed with the bytes of each of the data in such high byte link serial data;

an analyzer board adapted for plugging into the transmitter board, such analyzer board comprising:

a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board, and for converting the received low significant bytes of each data and the special characters interspersed therewith in the low byte serial link into corresponding lower significant bytes in a parallel low byte link and concurrently converting the received higher significant bytes in each data and the special characters interspersed therewith in the ~~low~~ high byte serial link into corresponding parallel higher significant bytes in a parallel high byte link;

a system for determining whether the data and pattern of special characters in the parallel low byte link matches the data and the pattern of special characters in the parallel high byte link, a determined match indicating the high byte parallel link is aligned with the low byte parallel link and a mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches, such system providing a reset signal when a predetermined plurality of mismatches has been indicated; and

wherein the reset signal is fed to the serializer-deserializer to reset such serializer-deserializer.

5. (original) An interface, comprising:

a plurality of director boards;

a plurality of memory boards, each one of the director boards being connected to the plurality of memory boards with a corresponding one of a plurality of point-to-point serial bus primary channels, a director board-to-memory board portion of each one of such primary channels passing signals from such one of the director boards and the corresponding one of the memory boards and a memory board-to-director board portion of each one of such primary channels passing signals from such corresponding one of the memory boards to such one of the director boards;

a plurality of adapter boards, each one being connected to a corresponding one of the director boards, each one of the plurality of adapter boards receiving a copy of signals from the director board-to-memory board portion of each one of such

primary channels passing signals from the one of the director boards connected thereto and receiving a copy of signals from the a memory board-to-director board portion of each one of such primary channels passing signals from the corresponding one of the director boards connected thereto, the copy of the memory board-to-director board portion having a high byte serial link and a low byte serial link and the copy of the memory board-to-director board portion having a high byte serial link and a low byte serial link;

a plurality of analyzer boards, each one being pluggable into a corresponding one of the adapter boards, each one of such analyzer boards, comprising:

a serializer-deserializer for converting:

the copy of the memory board-to-director board portion having the low byte serial link into a low byte parallel link representing the low byte serial link of the copy of the memory board-to-director board portion;

the copy of the memory board-to-director board portion having the high byte serial link into a high byte parallel link representing the high byte serial link of the copy of the memory board-to-director board portion;

the copy of the director board-to-memory board portion having the low byte serial link into a low byte parallel link representing the low byte serial link of the copy of the director board-to-memory board portion; and

the copy of the memory board-to-director board portion having the high byte serial link into a high byte parallel link representing the high byte serial link of the copy of the director board-to-memory board portion;

a logic for determining:

whether the low byte parallel link representing the copy of the memory board-to-director board portion is aligned with the high byte

parallel link representing the copy of the memory board-to-director board portion; and

whether the low byte parallel word representing the copy of the director board-to-memory board portion is misaligned with the high byte parallel link representing the copy of the director board-to-memory board portion;

such logic producing a reset signal if such logic determines either:

the low byte parallel link representing the copy of the memory board-to-director board portion is misaligned with the high byte parallel link representing the copy of the memory board-to-director board portion; or

the low byte parallel link representing the copy of the director board-to-memory board portion is misaligned with the high byte parallel link representing the copy of the director board-to-memory board portion; and

wherein such reset signal is fed to the serializer-deserializer to reset such serializer-deserializer.

6. (original) The interface recited in claim 5 wherein:

the copy of the director board-to-memory board portion has in the high byte serial link thereof special characters interspersed in a pattern with the data in the high byte serial link thereof and has in the low byte serial link thereof special characters interspersed in a pattern with the data in the low byte serial link thereof;

the copy of the director board-to-memory board portion has in the high byte serial link thereof special characters interspersed in a pattern with the data in the high byte serial link thereof and has in the low byte serial link thereof special characters interspersed in a pattern with the data in the low byte serial link thereof;

the serializer-deserializer:

converts the copy of the director board-to-memory board portion high byte

serial link and the special characters interspersed with the data in the high byte serial link thereof into corresponding parallel higher significant bytes of the high byte parallel link thereof and concurrently converts the copy of the director board-to-memory board portion low byte serial link and the special characters interspersed with the data in the low byte serial link thereof into corresponding parallel lower significant bytes of the low byte parallel link thereof;

converts the copy of the memory board-to-director board portion high byte serial link and the special thereof characters interspersed the data in the high byte serial link thereof into corresponding parallel higher significant bytes of the high byte parallel link thereof and concurrently converts the copy of the director board-to-memory board portion low byte serial link and the special characters interspersed with the data in the low byte serial link thereof into corresponding parallel lower significant bytes of the low byte parallel link thereof.

7. (original) The interface recited in claim 6 wherein the logic determines whether the data and pattern of special characters in the converted low byte parallel link and the data and the pattern of special characters in the converted high byte parallel link for the memory board-director board portion are misaligned and whether the data and pattern of special characters in the converted low byte parallel link and the data and the pattern of special characters in the converted high byte parallel link for the director board-memory board portion are misaligned.

8. (original) The interface recited in claim 7 wherein such system maintains a count of the number of mismatches, such system providing a reset signal when a predetermined plurality of mismatches has been indicated.

9. (original) The interface recited in claim 8 wherein:

each one of the adapter boards has a connector with a linear array of N pins, such pins being arranged in sets of four pins, each set of four pins for the copy of signals from the director board-to-memory board portion of each one of such primary channels passing signals

and the copy of signals from the a memory board-to-director board portion of each one of such primary channels passing signals to provide N/4 redundant channels, where N is an integer greater than one; and

each one of the analyzer boards has a connector with a linear array of M pins adapted for connecting to the connector of a corresponding one of the adapter board connectors,, where M =N/2, such analyzer board pins being arranged in sets of four pins, each set of four pins providing a receiving channel, such adapter board pins thereby providing M/4 receiving channels, each one of the M/4 receiving channels being adapted for connection to a corresponding one of the N/4 redundant channels thereby providing connections to N/2 redundant channels and N/2 unconnected redundant channels, one of the M/4 receiving channels being connected one of the redundant channels disposed adjacent to one of the unconnected redundant channels.